CS-99-063B

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February 12, 2003

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/077,093 02/19/02

Subhash Gupta et al.

METHOD TO FORM SELF-ALIGNED, L-SHAPED SIDEWALL SPACERS

Grp. Art Unit: 2812

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on February 13, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 2/13/03

This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Action under 1.113 or Notice of Allowance under 1.311 (37CFR 1.97(c)).

European Patent Application 0 227 303 A2 to Kenny et al., "Method of manufacturing semiconductor devices having side-wall isolation," discusses a method in which a silicon or polysilicon feature and overlayer of deposited dielectric is protected by a covering layer of nitride, a layer of polysilicon is deposited and is treated to define a sidewall fillet of oxide.

U.S. Patent 5,817,562 to Chang et al., "Method for Making Improved Polysilicon FET Gate Electrode Structures and Sidewal Spacers for More Reliable Self-Aligned Colntact (SAC)," discloses a method for making FET stacked gate electrode structures with improved sidewall profiles.

European Patent Application EP 0 951 061 A2 to Badenes et al., "Method for forming a FET," discloses a scaleable device concept and particularly a method for fabrication thereof.

French Patent Application 2 760 130 to Marty Michel et al., "MOS Transistor Having Low Drain Resistance," discloses a MOS transistor having from each side of its gate L-shaped spacers with the vertical part of the "L" resting against the gate.

U.S. Patent 5,895,955 to Gardner et al., "MOS Transistor Employing a Removable, Dual Layer Etch Stop to Protect Implant Regions from Sidewall Spacer Overetch," discloses a transistor and transistor fabrication method where a sequence of layers are formed and either entirely or partially removed upon sidewall surfaces of a gate conductor.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761